

65

ISSUE
2D

AT&TCO
STANDARD

CPS-JK8
3 SHEETS

BUS TERMINATOR A CIRCUIT



PART OF CPS JK8

BUS TERMINATOR A CIRCUIT

COMPONENT LIST

INTEGRATED CIRCUIT

LOC CODE ELEM	IC2 410B		IC4 410P		IC6 410A		IC7 410A		IC8 410E		IC10 410		IC11 410		IC12 410E		IC13 410P		IC14 410P		IC15 410	
ID	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	SP01	2C9	SP01	2B5	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1
B	0811	2B1	CL080	2B6	DVCOO	2C9	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1
C	2431	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1
D	0541	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1
E			SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1
F			CL081	2C6	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1
G			SP01	2C5	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1	SP01	2B1

LOC CODE ELEM	IC16 410	IC18 410E	IC19 410A	IC20 410E
ID	DESIG	SH LOC	DESIG	SH LOC
A	SP01	2B5	SP01	2B1
B	SP01	2B1	SP01	2B1
C	SP01	2B1	SP01	2B1
D	SP01	2B1	SP01	2B1
E	SP01	2B1	SP01	2B1
F	SP01	2B1	SP01	2B1
G	SP01	2B1	SP01	2B1

CAPACITOR

DESIG	CODE
(15) C1-C15	KS-19774 L5,0.1
(4) C16-C19	601A,5

RESISTOR

DESIG	CODE
(6) R1-R6	KS-20616 L1A,182
(11) R7-R17	301
(6) R18-R23	182
(11) R24-R38	392
(6) R39-R43	243
(11) R44-R51	345
(6) R52-R57	160
(11) R58-R64	301
(6) R65-R70	345

CIRCUIT DESCRIPTION

THIS CIRCUIT PACK IS PART OF THE BUS TERMINATOR DEVICE. HANDSHAKING AND CONTROL LOGIC FOR THE PARALLEL HOLDING REGISTER IN JK8 IS PROVIDED. PARALLEL HOLDING REGISTER FOR THE PARALLEL BUS COMMAND LEADS AND THE SERIAL BUS LEADS ARE ALSO PROVIDED.

THE BUS TERMINATOR ADDRESS FF (B7A0) BECOMES SET AT THE LEADING EDGE OF RCO AND IF B7A01 THROUGH B7A04 ARE ALL ONE'S OR ALL ZERO'S, RCO1 AND RCO4 ASSERT SYNC AND CLEARD. SYNC AND CLEARD REMAIN LOW UNTIL RCO RETURNS TO A HIGH LEVEL. AT THE TRAILING EDGE OF RCO, THE STATE OF THE INFORMATION LEADS IS Clocked INTO THE REGISTER IN JK9.

A LOW LEVEL IN RCO AND FF B7A0 BEING SET ASSERTS SYNC AND CLEARD. SYNC REMAINS LOW UNTIL RCO RETURNS TO A HIGH LEVEL. AT THE TRAILING EDGE OF RCO, THE STATE OF THE INFORMATION LEADS IS Clocked INTO THE REGISTER IN JK9.

A LOW LEVEL IN S50 AND FF B7A0 BEING SET ASSERTS SYNC AND CLEARD. CLEARD GATES THE OUTPUTS OF THE REGISTER IN JK9 INTO THE INFORMATION LEADS.

COMMAND INPUTS INITG IN ACKIO ASSERT SYNC. INITG IS ASSERTED BY ETCH1. FF5 A7A0, AND GATE AICLO GENERATE A CLOCK PULSE IN CLEARD. THE TRAILING EDGE OF THIS PULSE CLOCKS THE STATE OF THE INFORMATION LEADS INTO THE REGISTER IN JK9. THE TRAILING EDGE OF CLEARD1 Toggles FF S50 ENABLING THE TIMING CHAIN. FF5 DA AND DB TO ASSERT GPO AND GPO1. WHEN FF DB BECOMES SET WAITO IS NEGATED. GPO, GPO1, AND SYNC REMAIN TRUE UNTIL INITG IN ACKIO RETURN TO A HIGH LEVEL.

A PULSE IN THE GPO LEAD, WHILE S50 IN S50 IS LOW, ENABLES THE TIMING CHAIN S50, DA, AND DB. THE LEADING EDGE OF GPO ASSERTS WAITO. AT THE TRAILING EDGE OF GPO, THE PARALLEL REGISTER IN JK9 IS Clocked VIA CLEARD AND FF S50 IS Toggled. THE NEXT TRANSITION OF THE CLOCK Toggles FF DA. THE ONE PUT-PUT BY FF DA ASSERTS GPO AND ENABLES THE OUTPUTS OF THE REGISTER IN JK9 VIA GPO1. THE NEXT TRANSITION OF THE INVERTED CLOCK (CLEARD1) Toggles FF DB AND WAITO IS NEGATED. GPO1 AND GPO REMAIN TRUE UNTIL S50 IN S50 RETURN TO A HIGH LEVEL.

2D1

JK8 CIRCUIT PACK

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CPS-JK8
SHEET 3

BELL TELEPHONE LABORATORIES
UNIVERSITY MICROFILMS

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